IN THE CLAIMS:

Please enter the following claims (claims 1-12)

1. (Currently Amended) A memory array comprising:

a plurality of single-ended, dual-port, destructive-write memory cells arranged in an array formation of rows and columns, each cell having a read port consisting of a read data terminal and a read activation terminal, and further a write port consisting of a write data terminal and a write activation terminal, the read data terminal being accessed by asserting the cell read activation terminal and the write data terminal being accessed by asserting the cell write activation terminal,

wherein in each column of cells, a read bitline connects all the read data terminals of each cell, each read bitline having a read sense amplifier connected thereto, and a write bitline with an associated write data driver connected to the write data terminal of the memory cells, and

wherein when the read activation terminal is asserted, the read data terminal presents data depending upon the stored content of the memory cell, and when the write activation terminal is asserted, the content of the memory cell is set according to the state of the write data terminal; and

a circuit associated with each of the read sense amplifiers and each of the write data drivers for holding data sensed by the read sensing amplifier, making data read by the read sense amplifier available to the write data driver.

2. (cancelled)

3. (Original) The memory array as recited in claim 2, wherein depending on electrical signals generated outside the memory array, the circuit combines data read out from the read sense amplifier and data received from outside the memory array to make it available to the write data driver.

4. (Original) The memory array as recited in claim 1, wherein the write wordlines are coupled to the write activation terminals of the memory cells, the write wordlines being positioned orthogonally to the read and write bitlines, and wherein the plurality of read wordlines are connected to the read activation terminals of the memory cells and positioned orthogonally to the read and write bitlines.

5. (Original) The memory array as recited in claim 3, wherein the read and write wordlines are asserted by a wordline decoder and by corresponding write data drivers, and wherein one read wordline and one write wordline are asserted simultaneously for different cells of the memory array.

6. (Original) The memory array as recited in claim 3, wherein the circuit associated with each read sense amplifier and write data driver holds data sensed by the read sensing amplifier, providing a means for allowing data read-out of the array during one cycle to be modified and written-back to the memory array concurrently with the read-out operation of the next memory cycle.

7. (Original) The memory array as recited in claim 6, wherein the write cycle consists of read-out and write-back phases.

8. (Original) The memory array as recited in claim 3 wherein selected bits of the data read-out are modified by input data provided from outside the memory array before being written-back during a write cycle.

9. (Original) The memory array as recited in claim 3 further comprises an output data terminal wherein selected bits of the read-out data are outputted to outside the memory array.

10. (Original) The memory array as recited in claim 3, wherein circuit elements connect each read sense amplifier to a corresponding write data driver to provide means for refreshing the memory cells.

11. (Original) The memory array as recited in claim 3, wherein a circuit is provided with each row decoder circuit to activate corresponding write wordlines during the write-back phase of a cycle occurring concurrently with the activation of a read wordline.

12. (Original) The memory array as recited in claim 3, wherein the write wordline circuit is a latch connected to a driver

13. (Original) The memory array as recited in claim 3, wherein the write wordline is activated by a delayed clock

14. (Original) The memory array as recited in claim 9, wherein the columns to be read out of the memory array and written into the memory array are selected by a column decoder.

15. (Original) The memory array as recited in claim 14, wherein the column decoder activates a column read switch which connects selected read sense amplifiers to the output terminal of the memory array.

16. (Original) The memory array as recited in claim 14, wherein the column decoder activates a column write switch connecting the memory input port to the write data drivers allowing the selected write data to override data from the read sense amplifier.

17. (Original) The memory array as recited in claim 16, wherein activation of the column write switch is triggered by the delayed clock.

18. (Original) The memory array as recited in claim 1, wherein the memory cells are read-out non-destructively.

19. (Original) The memory array as recited in claim 1, wherein the memory cells are read-out destructively.

20. (Original) The memory array as recited in claim 3, further comprising an address match detection means for detecting when a write cycle is immediately followed by a read cycle at the same address, wherein during a pipelined operation, the read cycle overlaps with a previous write cycle, and wherein when addresses of two operations coincide, input data associated with a write operation and modified by logic operations associated with the latch and the multiplexer is delivered to the memory array output data port.

21. (Original) The memory array as recited in claim 3, wherein the sense amplifiers are single-ended, current mode sense amplifier.

22. (Original) The memory array as recited in claim 3, wherein the sense amplifiers are differential amplifiers.

23. (Original) The memory array as recited in claim 3, wherein a pipeline operation is controlled by at least one clock.

24. (Original) The memory array as recited in claim 3, wherein the memory cells are selected from the group of cells consisting of 3-transistors and 1-capacitor (3T 1C); 2-transistors and 1-capacitor (2T 1C); and 1-transistor and 1-capacitor (1T 1C).